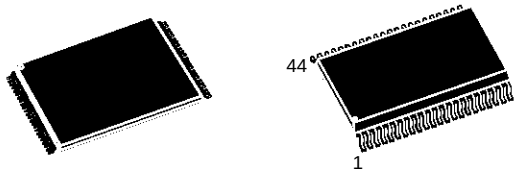
SGS-THOMSON MICROELECTRONICS

M29F400T
M29F400B

SINGLE SUPPLY
4 Megabit (x8/x16, Block Erase) FLASH MEMORY

PRODUCT PREVIEW

- DUAL x8 and x16 ORGANISATION
- FAST ACCESS TIME: 70ns
- 5V±10% SUPPLY VOLTAGE for PROGRAM/ERASE and READ OPERATIONS
- TYPICAL PROGRAMMING TIME
  - 10µs by Byte/16µs by Word
- PROGRAM/ERASE CONTROLLER (P/E.C.)
  - Program Byte-by-Byte/Word-by-Word
  - Data polling and Toggle Protocol for P/E.C. Status
  - Ready/Busy Pin
  - Hardware Reset Pin
- MEMORY ERASE in BLOCKS
  - One 16K Byte Boot Block (Top or Bottom location) with hardware write and erase protection
  - Two 8K Byte (4K Word) Parameter Blocks
  - One 32K Byte (16K Word) Main Block
  - Seven 64K Byte (32K Word) Main Blocks
  - Multi Block Protection/Temporary Unprotection
  - Chip Erase
- ACCESS WORD CONFIGURATION BY PIN ($\overline{BYTE}$)
- ERASE SUSPEND AND RESUME MODES
  - Read and Program another Block during erase suspend
- LOW POWER CONSUMPTION
  - Active mode: 20mA typical Current for Read in Byte Mode
  - 28mA typical Current for Read in Word Mode
  - 30mA typical Current for Write/Erase
  - 25µA typical Current for Stand-by Mode
  - Automatic CMOS Stand-by mode
- 100,000 PROGRAM/ERASE CYCLES per BLOCK



TSOP48 (N)
12 x 20 mm

SO44 (M)

Figure 1. Logic Diagram

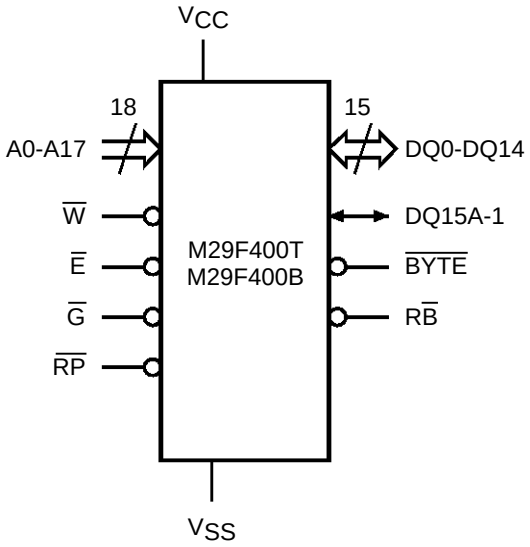


Figure 2A. TSOP Pin Connections

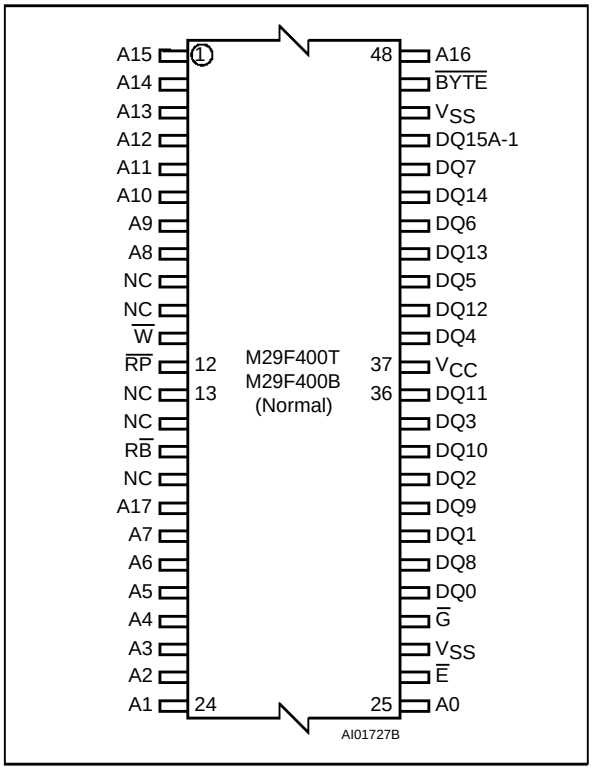


Figure 2B. TSOP Reverse Pin Connections

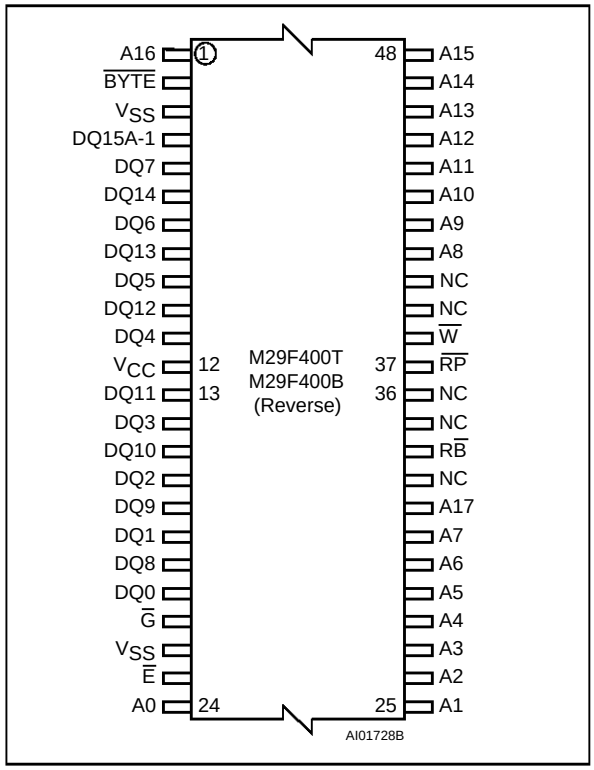


Figure 2C. SO Pin Connections

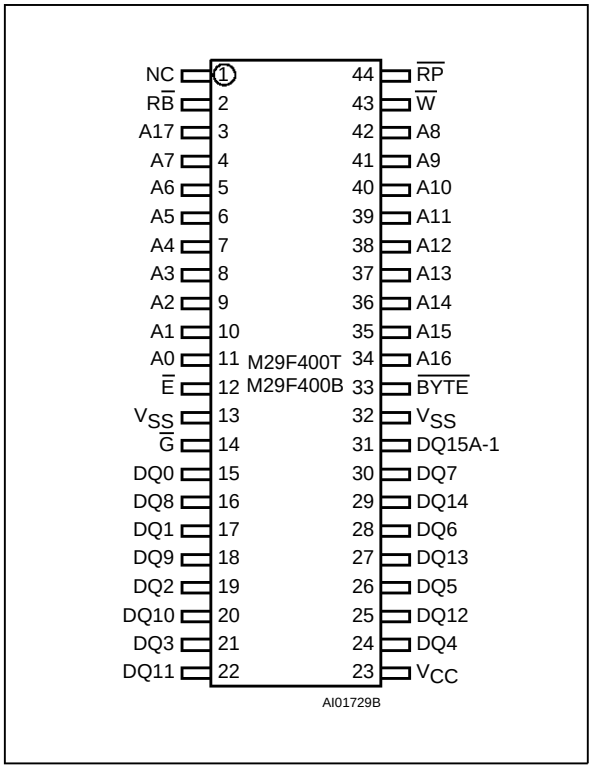


Table 1. Signal Names

A0-A17	Address Inputs
DQ0-DQ7	Data Input / Outputs
DQ8-DQ14	Data Input / Outputs
DQ15A-1	Data Input / Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Boot Block Unlock
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organisation
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9} (2)	A9 Voltage	–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

DESCRIPTION

The M29F400 is a non-volatile memory that may be erased electrically at the block level and programmed in-system on a Byte-By-Byte or Word-By-Word basis using the 5V V_{CC} supply. The device can also be programmed in standard EPROM programmers. The Sectorization allows each block to be erased and reprogrammed without affecting other blocks. The M29F400 is shipped erased from the factory.

The memory features single 5V ± 10% range voltage for both Read and Write operations. Commands are written to the Command Interface using standard microprocessor write timings. For Program and Erase cycles the voltages are generated and provided internally. Once the end of a program or erase cycle has been completed, the device internally resets to the Read mode. The M29F400 electrically erases the entire chip or all bits within a block simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed on single Byte or Word basis via the hot electron injection mechanism.

The interface is directly compatible with most microprocessors. TSOP48 and SO44 packages are offered. Both forward and reverse pinouts are available for the TSOP48 package.

Organisation

The M29F400 is organised as 512Kx8 or 256Kx16 bits with Address lines A0-A17 and Data Inputs/Outputs DQ0-DQ14. The organisation is selectable by an external $\overline{BYTE}$ signal. When $\overline{BYTE}$ is Low the x8 organisation is selected and the Data Input/Output signal DQ15 acts as Address line A-1.

The level on DQ15A-1 then selects the lower or upper byte of the memory word for output on DQ0-DQ7, DQ8-DQ14 remain high impedance. When $\overline{BYTE}$ is High the memory uses the Address inputs A0-A17 and the Data Input/Outputs DQ0-DQ15. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Block unlock, tri-level input, enables programming and erasure of the Blocks previously protected.

Erase and Program are performed through the internal Program/Erase Controller (P/E.C.).

Data Output bit DQ7 provides a data polling signal, and Data Outputs bits DQ6 and DQ2 provide toggle signals during Automatic Program or Erase to indicate the Ready/Busy state of the internal Program/Erase Controller and during Erase Suspend to indicate the Read or Program of another block (if performed).

Blocks

The device features an asymmetrically blocked architecture providing system memory integration. Erasure can be performed in chip erase and block erase with any combination of the blocks. There are 11 blocks in the memory address space, one Boot Block of 16K Bytes or 8K Words, two Parameter Blocks of 8K Bytes or 4K Words, one Main Block of 32K Bytes or 16K Words and seven Main Blocks of 64K Bytes or 32K Words. The M29F400T has the Boot Block at the top of the memory address space and the M29F400B locates the Boot Block starting at the bottom. The memory maps are showed in Figure 5. Each block can be programmed and erased over 100,000 cycles.

Any combination of blocks can be protected and unprotected against program and erase. Block protection is obtained by putting 10.5V on A9 and $\overline{G}$ and then providing the block address.

Table 3. User Bus Operations (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{BYTE}$	A0	A1	A6	A9	DQ0-DQ7	DQ8-DQ14	DQ15A-1
Read Word	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	A0	A1	A6	A9	Data Output	Data Output	Data Output
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	A0	A1	A6	A9	Data Output	Hi-Z	Address Input
Write Word	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	A0	A1	A6	A9	Data Input	Data Input	Data Input
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	A0	A1	A6	A9	Data Input	Hi-Z	Address Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z
Block Protection Setup (2)	V_{IL}	V_{ID}(4)	Pulse/H (3)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}(4)	X	X	X
Block Protection Verify (2)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}(4)	Code(5)	X	X
Block Temporary Unprotection	X	X	X	V_{ID}(4)	X	X	X	X	X	X	X	X

Notes: 1. X = V_{IL} or V_{IH}
2. Address Block must be given on A12-A17 bits.
3. Pulse/H = $\overline{W}$ pulse with latching on rising edge.
4. V_{ID} from 11.5V to 12.5V.
5. Code = '00' for Unprotected Block, '01' for Protected Block.

Table 4. Electronic Signature

Organi-sation	Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{BYTE}$	A0	A9	A1-A8 & A10-A17	DQ0 - DQ7	DQ8 - DQ14	DQ15 A-1
Word-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{ID}	Don't Care	20h	00h	0
	Device Code	M29F400T	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0D5h	00h	0
		M29F400B	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0D6h	00h	0
Byte-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h	Hi-Z	Don't Care
	Device Code	M29F400T	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{ID}	Don't Care	0D5h	Hi-Z	Don't Care
		M29F400B	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{ID}	Don't Care	0D6h	Hi-Z	Don't Care

Note: $\overline{RP}$ = V_{IH}

Table 5. Block Protection Status

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A12	A13	A14	A15	A16	A17	Other Addresses	DQ0 - DQ7
Protected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	SA	SA	SA	Don't Care	01h
Unprotected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	SA	SA	SA	Don't Care	00h

Note: SA = Address of Block being checked.

Bus Operations

Seven operations can be performed by the appropriate bus cycles, Read Array, Read Electronic Signature, Output Disable, Standby, Block Erase Suspend and Resume, Reset, Write the Command of an Instruction.

Command Interface

Command Bytes can be written to a Command Interface latch (C.I.) to perform Reading (from the Array or Electronic Signature), Erasure or Programming. For added data protection, command execution starts after 4 or 6 command cycles. The first, second, fourth and fifth cycles are used to input a code sequence to the Command Interface (C.I.). This sequence is equal for all P/E.C. instructions. 'Command' itself and its confirmation, it applicable, are given on the third and fourth or sixth cycles. Any incorrect Command Byte or any improper Command Bytes sequence will put the device directly in Read Mode.

Instructions

Seven instructions are defined to perform Read Memory Array, Read Electronic Signature, Auto Program, Block Auto Erase, Auto Chip Erase, Block Erase Suspend and Block Erase Resume. The internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides Data Polling, Toggle and Status Data to indicate completion of Program and Erase Operations.

Instructions are composed of up to six cycles. The first two cycles input a code sequence to the Command Interface which is common to all P/E.C. instructions (see Table 7 for Command Descriptions). The third cycle inputs the instruction set-up command to the Command Interface. Subsequent cycles output Signature, Block protection or the addressed data for Read operations. In order to give additional data protection, the instructions for program and Block or bulk erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For an Erase instruction (block or chip), the fourth and fifth cycles input a further code sequence before the Erase confirm command on the sixth cycle. Byte programming takes typically 10µs, Word Programming takes typically 16µs. Block erase is performed in typically 1.5 seconds for the main blocks (64Kb).

Erasure of a memory block may be suspended, in order to read data from another block or to program data in another block, and then resumed. Data Polling, Toggle ($R\overline{B}$ pin) and Error data may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. When power is first applied or if Vcc falls below V_{LKO}, the command interface is reset to Read Array.

DEVICE OPERATION

Signal Descriptions

A0-A17 Address Inputs. The address inputs for the memory array are latched during a write operation. The A9 address input is used also for the Electronic Signature read and Block Protect verification. When A9 is raised to V_{ID}, either a Read Manufacturer Code, Read Device Code or Verify Block Protection is enabled depending on the combination of levels on A0, A1 and A6. When A0, A1 and A6 are Low, the Electronic Signature Manufacturer code is read, when A0 is High and A1 and A6 are Low, the Device code is read, and when A1 is High and A0 and A6 are low, the Block Protection Status is read for the block addressed by A12, A13, A14, A15, A16, A17.

Table 6. Instructions (1, 2)

Mne.	Instr.	Cyc.			1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RD (4)	Read/Reset Memory Array	1+	**Addr.** (3,7)		X	Read Memory Array until a new write cycle is initiated.					
			Data		0F0h						
RD (4)	Read/Reset Memory Array	3+	**Addr.** (3,7)	**Word**	x5555h	x2AAAh	x5555h	Read Memory Array until a new write cycle is initiated.			
				Byte	xAAAAh	x5555h	x2AAAh				
			Data		0AAh	55h	0F0h				
RSIG (4)	Read Electronic Signature	3+	**Addr.** (3,7)	**Word**	x5555h	x2AAAh	x5555h	Read Electronic Signature until a new write cycle is initiated. See Note 5.			
				Byte	xAAAAh	x5555h	x2AAAh				
			Data		0AAh	55h	90h				
RBP (4)	Read Block Protection	3+	**Addr.** (3,7)	**Word**	x5555h	x2AAAh	x5555h	Read Block Protection until a new write cycle is initiated. See Note 6.			
				Byte	xAAAAh	x5555h	x2AAAh				
			Data		0AAh	55h	90h				
PG	Program	4	**Addr.** (3,7)	**Word**	x5555h	x2AAAh	x5555h	Program Address	Read Data Polling or Toggle Bit until Program completes.		
				Byte	xAAAAh	x5555h	x2AAAh				
			Data		0AAh	55h	0A0h	Program Data			
SE	Block Erase	6	**Addr.** (3,7)	**Word**	x5555h	x2AAAh	x5555h	x5555h	x2AAAh	Block Address	Additional Block (8)
				Byte	xAAAAh	x5555h	x2AAAh	x2AAAh	x5555h		
			Data		0AAh	55h	80h	0AAh	55h	30h	30h
BE	Bulk Erase	6	**Addr.** (3,7)	**Word**	x5555h	x2AAAh	x5555h	x5555h	x2AAAh	x5555h	Note 9
				Byte	xAAAAh	x5555h	x2AAAh	x2AAAh	x5555h	x2AAAh	
			Data		0AAh	55h	80h	0AAh	55h	10h	
ES (10)	Erase Suspend	1	**Addr.** (3,7)		X	Read until Toggle stops, then read all the data needed from any Block(s) not being erased then Resume Erase.					
			Data		0B0h						
ER	Erase Resume	1	**Addr.** (3,7)		X	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time					
			Data		30h						
PD	Power Down	1	**Addr.** (3,7)		X						
			Data		20h						

Notes: 1. Command not interpreted in this table will default to read array mode.
2. The user should generate the following address patterns:
in Word mode: x5555h or 2AAAAh to addresses A0-A14;
in Byte mode: AAAAh or x5555h to addresses A1-A14.
3. X = Don't Care.
4. The first cycle of the RD, RSP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of read cycles can occur after one command cycle.
5. Signature Address bits A0, A1, A6 at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, A6 at V_{IL} will output Device code (0D5h for the Top Boot, 0D6h for the Bottom Boot).
6. Protection Address: A0, A6 at V_{IL}, A1 at V_{IH} and A12, A13, A14, A15, A16 and A17 within the Block to be checked, will output the Block Protection status.
7. Address bits A12, A13, A14, A15, A16 and A17 are don't care for coded address inputs.
8. Optional, additional Blocks addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through DQ3 value. When full command is entered, read Data Polling or Toggle bit until Erase is completed or suspended.
9. Read Data Polling or Toggle bit until Erase completes.
10. During Erase Suspend, Read and Byte Program functions are allowed in blocks not erasing.

DQ0-DQ7 Data Input/Outputs. These Inputs/Outputs are used in the byte-wide organisation. The data input is a byte to be programmed or a command written to the C.I. Both are latched when Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output is from the memory Array, the Electronic Signature, the Data Polling bit (DQ7), the Toggle Bits (DQ6 and DQ2), the Error bit (DQ5) or the Erase Timer bit (DQ3). Ouputs are valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled and when $\overline{RP}$ is at a Low level.

DQ8-DQ14 and DQ15A-1 Data Input/Outputs. These Inputs/Outputs are used in the word-wide organisation. When $\overline{BYTE}$ is High DQ8-DQ14 and DQ15A-1 act as the most significant byte of the Input or Output, functioning as described for DQ0-DQ7 above. When $\overline{BYTE}$ is Low, DQ0-DQ14 are high impedance, DQ15A-1 is the Address A-1 input.

Table 7. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Chip Erase Confirm
20h	Power Down
30h	Block Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature/ Block protection Status
0A0h	Program
0B0h	Erase Suspend
0F0h	Read Array/Reset

Table 8. Status Register

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase On-going	
		DQ	Program Complete	
		$\overline{DQ}$	Program On-going	
6	Toggle Bit 1	'-1-0-1-0-1-0-1-'	Erase or Program On-going	Successive reads output complementary data on DQ6 while Programming or Erase operations are going on. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		'-0-0-0-0-0-0-0-'	Erase or Program ('0' on DQ6) Complete	
		'-1-1-1-1-1-1-1-'	Erase or Program ('1' on DQ6) Complete	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' if P/E.C. has exceeded the specified time limits.
		'0'	Program or Erase On-going	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES). An additional block to be erased in parallel can be entered to the P/E.C.
		'0'	Erase Timeout Period On-going	
2	Toggle Bit 2	'-1-0-1-0-1-0-1-'	Erase, Erase suspend (Erasing Block address) Erase suspend program	
		1	Program	
1	Program			
0	Reserved			

Notes: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Addresses are then latched on the falling edge of $\overline{E}$ while data is latched on the rising edge of $\overline{E}$. The Chip Enable must be forced to V_{ID} during Block Unprotect operations.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation. $\overline{G}$ must be forced to V_{ID} level during Block Protect and Block Unprotect operations.

$\overline{W}$ Write Enable. This input controls writing to the Command Register and Address and Data latches. Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

$\overline{BYTE}$. The $\overline{BYTE}$ Pin selects the output configuration for the device: byte (x8) mode or word (x16) mode. When the $\overline{BYTE}$ is Low, the 8 bit mode is selected and the data is read and programmed at DQ0-DQ7. Under this mode, DQ8-DQ14 are at high impedance and DQ15A-1 is the lowest address bit. When the $\overline{BYTE}$ is High, the 16 bit mode is selected and the data is read and programmed at DQ0-DQ15.

R$\overline{B}$ Ready/Busy Output Pin. The Ready/Busy pin is an open-drain output pin and shows the internal write state of the device. When R$\overline{B}$ is Low, the device is Busy with a Program or Erase operation and it will not accept any additional program or erase instructions. When R$\overline{B}$ is High, the device is ready for any Read/Write or Erase operation. The R$\overline{B}$ will also be High when the memory is put in Erase Suspend mode. During standby mode the R$\overline{B}$ pin is at high level.

$\overline{RP}$ Reset Pin. The Reset Pin provides a Reset function via hardware when it is Low. $\overline{RP}$ must be kept Low (V_{IL}) for at least 500ns. The memory will become ready for a read operation 15µs after the falling edge of the $\overline{RP}$. After bringing the Reset Pin to a High level, Read/Write operation is possible after an appropriate delay of 50ns. Any hardware reset during program or erase operation will corrupt the contents of the memory at that particular location.

Additionally, the $\overline{RP}$ pin provides protection against unwanted command writes due to invalid system bus conditions that may occur during system reset and power up/down sequences.

By putting $\overline{RP}$ at V_{ID}, the temporary block unprotection is allowed.

V_{CC} Supply Voltage. The power supply for all operations (Read, Program and Erase).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Memory Blocks

The memory blocks of the M29F400 are shown in Figure 5. The memory array is divided in 11 blocks: one Boot Block of 16K Bytes or 8K Words, two Parameter Blocks of 8K Bytes or 4K Words, one Main Block of 32K Bytes or 16K Words, seven Main Blocks of 64K Bytes or 32K Words. Each block can be erased separately or any combination of blocks can be erased simultaneously. The Block Erase operation is managed automatically by the P/E.C. The operation can be suspended in order to read from any other Block and then resumed.

Block Protection provides additional data security. Each block can be separately protected or unprotected against Program or Erase. Bringing A9 and $\overline{G}$ to V_{ID} initiates protection, while bringing A9, $\overline{G}$ and $\overline{E}$ to V_{ID} cancels the protection. The block affected during protection is addressed by the inputs on A12, A13, A14, A15, A16 and A17. The unprotect operation affects all blocks. The Boot Block does not need to be protected since it is hardware protected.

Operations

Operations are defined as specific bus cycles and signals which allow Memory Read, Command Write, Output Disable, Standby, Read Status Bits, Block Protect/Unprotect, Block Protection Check and Electronic Signature Read. They are shown in Tables 3, 4, 5.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RD and RSIG, and Status Bits).

Table 9. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

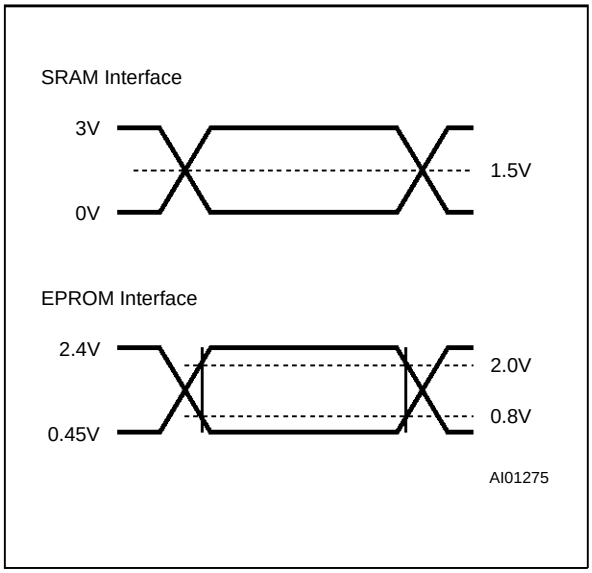


Figure 4. AC Testing Load Circuit

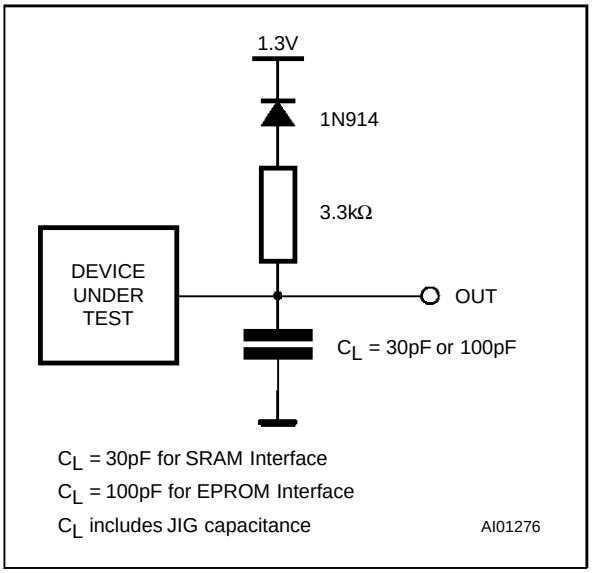


Table 10. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

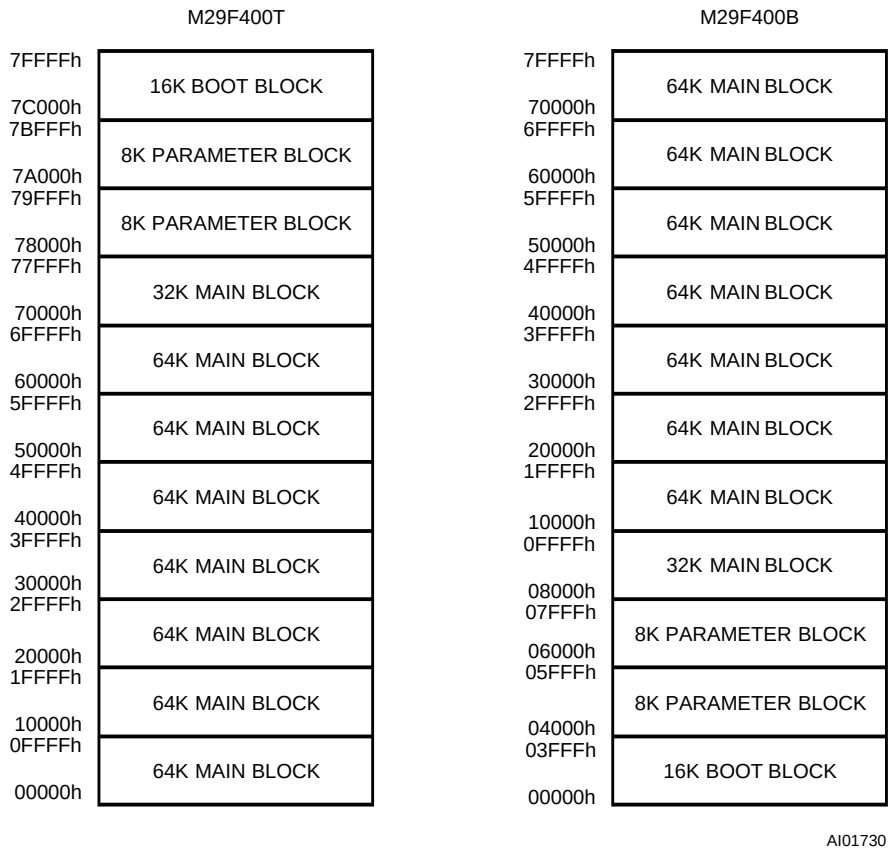
Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is High and Program/Erase Controller P./E.C. is Idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Automatic Standby. After 150ns of inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-standby mode where comsumption is reduced to the CMOS standby value, while outputs still drive the bus.

Figure 5. Memory Map and Block Address Table



Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory. The manufacturer's code for SGS-THOMSON is 20h, the device code is D5h for the M29F400T (Top Boot) and D6h for the M29F400B (Bottom Boot). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product. The Electronic Signature is output by a Read operation when the voltage applied to A9 is at V_{ID} and address inputs A1 and A6 are at Low. The manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0-DQ7. This is shown in Table 4.

The Electronic Signature can also be read, without raising A9 to V_{ID} by giving the memory the instruction RSIG (see below). If the byte-wide configuration is selected the codes are output on DQ0-DQ7 with DQ8-DQ14 at High impedance; if the word-wide configuration is selected the codes are output on DQ0-DQ7 with DQ8-DQ14 at 00h.

Block Protection. Each block can be separately protected against Program or Erase. Block Protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and $\overline{G}$ are set to V_{ID} and the block address is applied on A12, A13, A14, A15, A16 and A17. Block protection is programmed using a Presto F program- like algorithm. Protection is initiated on the edge of $\overline{W}$ falling to V_{IL}. Then after a delay of 100µs, the edge of $\overline{W}$ rising to V_{IH} ends the protection operations. Protection verify is achieved by bringing $\overline{G}$, $\overline{E}$ and A6 to V_{IL} while $\overline{W}$ is at V_{IH} and A9 at V_{ID}. Under these conditions, reading the data output will yield 01h if the block defined by the inputs on A12, A13, A14, A15, A16 and A17 is protected. Any attempt to program or erase a protected block will be ignored by the device.

Table 11. DC Characteristics
(T_A = 0 to 70°C, -20 to 85°C, -40 to 85°C or -40 to 125°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read) TTL Byte	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		40	mA
I_{CC1}	Supply Current (Read) TTL Word	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		50	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC4}	Supply Current (Program or Erase)	Byte program, Block or Bulk Erase in progress		60	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA		0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4V		V
		I_{OH} = –2.5mA	0.85 x V_{CC}		V
V_{ID}	A9 Voltage (Electronic Signature)		10.0	11.0	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		50	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		3.2	4.2	V

Block Temporary Unprotection. Any previously protected block can be temporarily unprotected in order to change stored data. The temporary unprotect mode is activated bringing $\overline{RP}$ to V_{ID}. During the temporary unprotection mode the previous protected blocks are unprotected. The block can be selected and data can be modified by executing the Erase or Program command with the pin held at V_{ID}. When V_{ID} is removed from the $\overline{RP}$ pin, all the previous protected blocks remain protected.

Block Unprotection. Any protected block can be unprotected to allow updating of bit contents. All blocks must be protected before an unprotect operation. Block unprotect is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID}. The addresses inputs A6 and A1 must be maintained at V_{IH}. Block unprotect is performed through a Presto F Erase-like algorithm. Unprotect is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the edge of $\overline{W}$ riding to V_{IH} will end the unprotection operation. Unprotect verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A6 and A1 are at V_{IH} and A9 at V_{ID}. In these conditions, reading the output data will yield 00h if the block defined by the inputs A12, A13, A14, A15, A16 and A17 has been succesfully unprotected. All combinations of A12, A13, A14, A15, A16 and A17 must be addressed in order to ensure that all of the 11 blocks have been unprotected. Block Protection Status is shown in Table 5.

Table 12A. M29F400T Block Address Table (x8 configuration)

Address Range	A17	A16	A15	A14	A13	A12
00000h-0FFFFh	0	0	0	X	X	X
10000h-1FFFFh	0	0	1	X	X	X
20000h-2FFFFh	0	1	0	X	X	X
30000h-3FFFFh	0	1	1	X	X	X
40000h-4FFFFh	1	0	0	X	X	X
50000h-5FFFFh	1	0	1	X	X	X
60000h-6FFFFh	1	1	1	X	X	X
70000h-77FFFh	1	1	1	0	X	X
78000h-79FFFh	1	1	1	1	0	0
7A000h-7BFFFh	1	1	1	1	0	1
7C000h-7FFFFh	1	1	1	1	1	X

Table 12B. M29F400B Block Address Table (x8 configuration)

Address Range	A17	A16	A15	A14	A13	A12
00000h-03FFFh	0	0	0	0	0	X
04000h-05FFFh	0	0	0	0	1	0
06000h-07FFFh	0	0	0	0	1	1
08000h-0FFFFh	0	0	0	1	X	X
10000h-1FFFFh	0	0	1	X	X	X
20000h-2FFFFh	0	1	0	X	X	X
30000h-3FFFFh	0	1	1	X	X	X
40000h-4FFFFh	1	0	0	X	X	X
50000h-5FFFFh	1	0	1	X	X	X
60000h-6FFFFh	1	1	1	X	X	X
70000h-7FFFFh	1	1	1	X	X	X

Instructions and Commands

The Command Interface (C.I.) latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Electronic Signature, Block Erase, Chip Erase, Program, Block Erase Suspend and Erase Resume. Commands are made of address and data sequences. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ and data is latched on the rising of $\overline{W}$ or $\overline{E}$. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the command. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of com-

Table 13A. Read AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)

Symbol	Alt	Parameter	Test Condition	M29F400				Unit
				-70 (4)		-90		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
				SRAM Interface		EPROM Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	70		90		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		90	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		20	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		20	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns
t_{READY} (1)		$\overline{RP}$ Low to Read Mode			20		20	µs
t_{ELBL} t_{ELBH}		Chip Enable to $\overline{BYTE}$ Switching Low or High			5		5	µs
t_{BLQZ} (3)		$\overline{BYTE}$ Switching Low to Output High Z			20		30	ns

Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
3. This timing is for temporary Sector Unprotection.
4. At grade 1 (0 to 70°C) temperature range.

mands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Commands are initialised by two preceding coded cycles which unlock the Command Interface. In addition, for Erase, command confirmation is again preceeded by the two coded cycles.

P/E.C. status is indicated during command execution by Data Polling on DQ7, detection of Toggle on DQ6 and DQ2, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt during Program or Erase command execution will automatically output these five bits. The P/E.C. automatically sets bits DQ2, DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1 and DQ4) are reserved for future use and should be masked.

Table 13B. Read AC Characteristics
(T_A = 0 to 70°C, -20 to 85°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	Test Condition	M29F400				Unit
				-120		-150		
				V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
				EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		55	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		35	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns
t_{READY} (1)		$\overline{RP}$ Low to Read Mode			20		20	µs
t_{ELBL} t_{ELBH}		Chip Enable to $\overline{BYTE}$ Switching Low or High			5		5	µs
t_{BLQZ} (3)		$\overline{BYTE}$ Switching Low to Output High Z			20		30	ns

Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
3. This timing is for temporary Sector Unprotection.

Data Polling Bit DQ7. When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid and only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. It must be performed at the address being programmed or at an address within the Block being erased. If the byte to be programmed belongs to a protected Block the command is ignored. If all the Blocks selected for erasure are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed memory data value. See Figure 9 for the Data Polling flowchart and Figure 10 for the Data Polling waveforms. DQ7 will also flag the Erase Suspend Mode by switching from '0' to '1' at the start of the Erase Suspend. In order to monitor DQ7 in the Erase Suspend Mode the address of an erasing block must be provided. During Program operation in Erase Suspend Mode, DQ7 will have the same behaviour as in the normal program execution outside of the suspend mode.

Toggle Bit 1 DQ6. When Programming operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either $\overline{G}$ or $\overline{E}$ when $\overline{G}$ is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit is valid only effective during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. If the byte to be programmed belongs to a protected block the command will be ignored. If the blocks selected for erasure are protected, DQ6 will toggle for about 100µs and then return back to Read. DQ6 will be set to '1' if a Read operation is attempted on an Erase Suspend Block. DQ6 will toggle driving a program operation in a block different to the block in Erase Suspend. Either $\overline{E}$ or $\overline{G}$ toggling will cause DQ6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ6 to toggle. See Figure 11 for Toggle Bit flowchart and Figure 12 for Toggle Bit waveforms.

Toggle Bit 2 DQ2. This toggle bit, together with DQ6, can be used to determine the chip status during the Erase Mode or Erase Suspend Mode. A Read operation will cause DQ2 to Toggle during the Erase Mode. If the chip is in Erase Suspend Mode, a Read operation from the Erase suspended block or a Program operation into the Erase suspend block will cause DQ2 to toggle. When the chip is in Program Mode during Erase Suspend, a Read Command from the byte address of a non-Erase Suspended block will set the DQ2 bit to a logic '1'. DQ2 has a differnt behaviour with respect to DQ6 which toggles only during the Standard Program or Erase, or Erase Suspend Program operation. See Table 14 for the behaviour of the two Toggle Bits DQ2 and DQ6, and of the Polling DQ7. DQ2 can also be used to identity the block being erased. DQ2 toggles when it is read from the block being erased.

Error bit DQ5. This bit is set to '1' by the P/E.C. when there is a failure of byte programming, erase, or chip erase that results in invalid data being programmed in the memory block. In case of an error in block erase or byte program, the block in which the error occured or to which the programmed byte belongs, must be discarded. The DQ5 failure condition will also appear if a user tries to program a '1' to a location that is previously programmed to '0'. Other Blocks may still be used. The error bit resets after Read/Reset (RD) instruction. In case of success, the error bit will set to '0' during Program or Erase and to indicate valid data after write operation is completed.

Table 14. Toggle Bit 2 DQ2

Mode	DQ7	DQ6	DQ2
Program	$\overline{DQ7}$	Toggle	1
Erase	0	Toggle	Toggle
Erase Suspend Read (1) (in Erase Suspend Block)	1	1	Toggle
Erase Suspend Program	$\overline{DQ7}$ (2)	Toggle	Toggle

Notes: 1. These status flags apply when outputs are read from a block that has been erase-suspended.
2. These status flags apply when outputs are read from the byte address of the non-erase suspended block.

Erase Timer bit DQ3. This bit is set to '0' by the P/E.C. when the last block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the wait period is finished, after 80µs to 120µs, DQ3 returns back to '1'.

Coded Cycles. The two coded cycles unlock the Command Interface. They are followed by a command input or a command confirmation. The coded cycles consist of writing the data 0AAh at address AAAAh in the Byte wide configuration and at address 5555h in the Word wide configuration during the first cycle. During the second cycle the coded cycles consist of writing the data 55h at address 2AAAAh in the Byte wide configuration and at address 25555h in the Word wide configuration. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ while data is latched on the rising edge of $\overline{W}$ or $\overline{E}$. The coded cycles happen on first and second cycles of the command write or on the fourth and fifth cycles.

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0F0h. It can be optionally preceded by the two coded cycles. Subsequent read operations will read the memory array addressed and output the read byte.

Read Electronic Signature (RSIG) instruction. This instruction uses the two coded cycles followed by one write cycle giving the command 90h to address 5555h for command setup. A subsequent read will output the manufacturer code, the device code or the Block protection status depending on the levels of A0, A1, A6, A16, A17 and A18. The manufacturer code, 20h, is output when the addresses lines A0, A1 and A6 are Low, the device code, 0D5h for Top Boot, 0D6h for bottom Boot is output when A0 is High with A1 and A6 Low.

Figure 6. Read Mode AC Waveforms

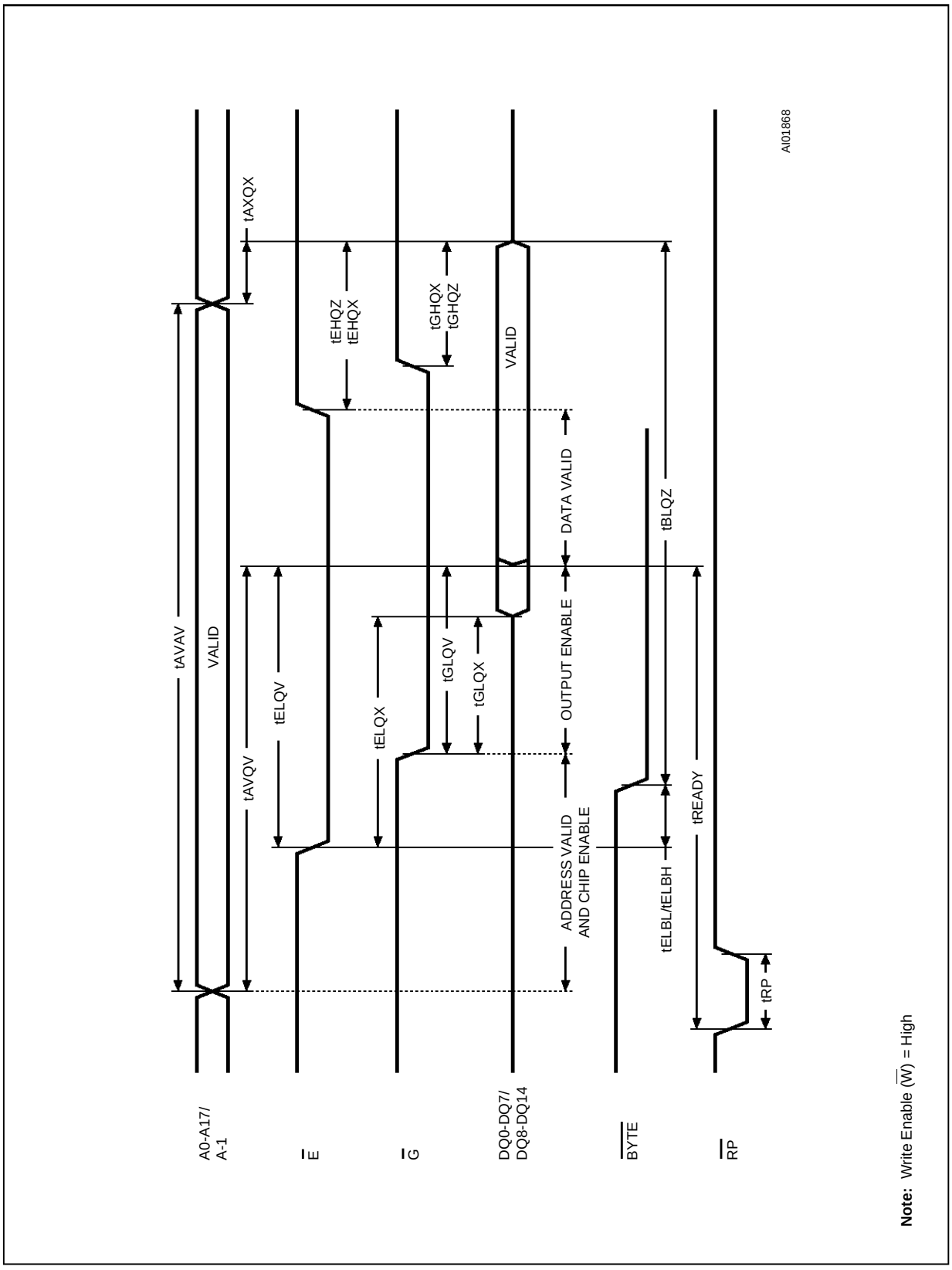


Table 15A. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, -20 to 85°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F400				Unit
			-70 (4)		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	35		45		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	30		45		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		45		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	10		10		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Block Erase)	1.5	30	1.5	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{VIDR} (2,3)		Rise TIme to V_{ID}	500		500		ns
t_{RP}		RP Pulse Width	500		500		ns
t_{BUSY} (2)		Program Erase Valid to $R\overline{B}$ Delay	30		35		ns

Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$
2. Not 100% tested.
3. These timing are for Temporary Block Unprotected operation.
4. At grade 1 (0 to 70°C) temperature range.

Read Block Protection (RBP). The use of Read Electronic Signature (RSIG) command also allows access to the block protection status verify. After giving the RBIG command, A0 and A6 are set to V_{IL} with A1 at V_{IH}, while A12, A13, A14, A15, A16 and A17 define the block of the block to be verified. A read in these conditions will output a 01h if block is protected and a 00h if block is not protected.

Chip Erase (CE) instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written to address 5555h on third cycle after the two coded cycles. The Bulk Erase Confirm command 10h is written at address 5555h on sixth cycle after another two coded cycles. If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts and the

Table 15B. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, -20 to 85°C, -40 to 85°C or -40 to 125°C)

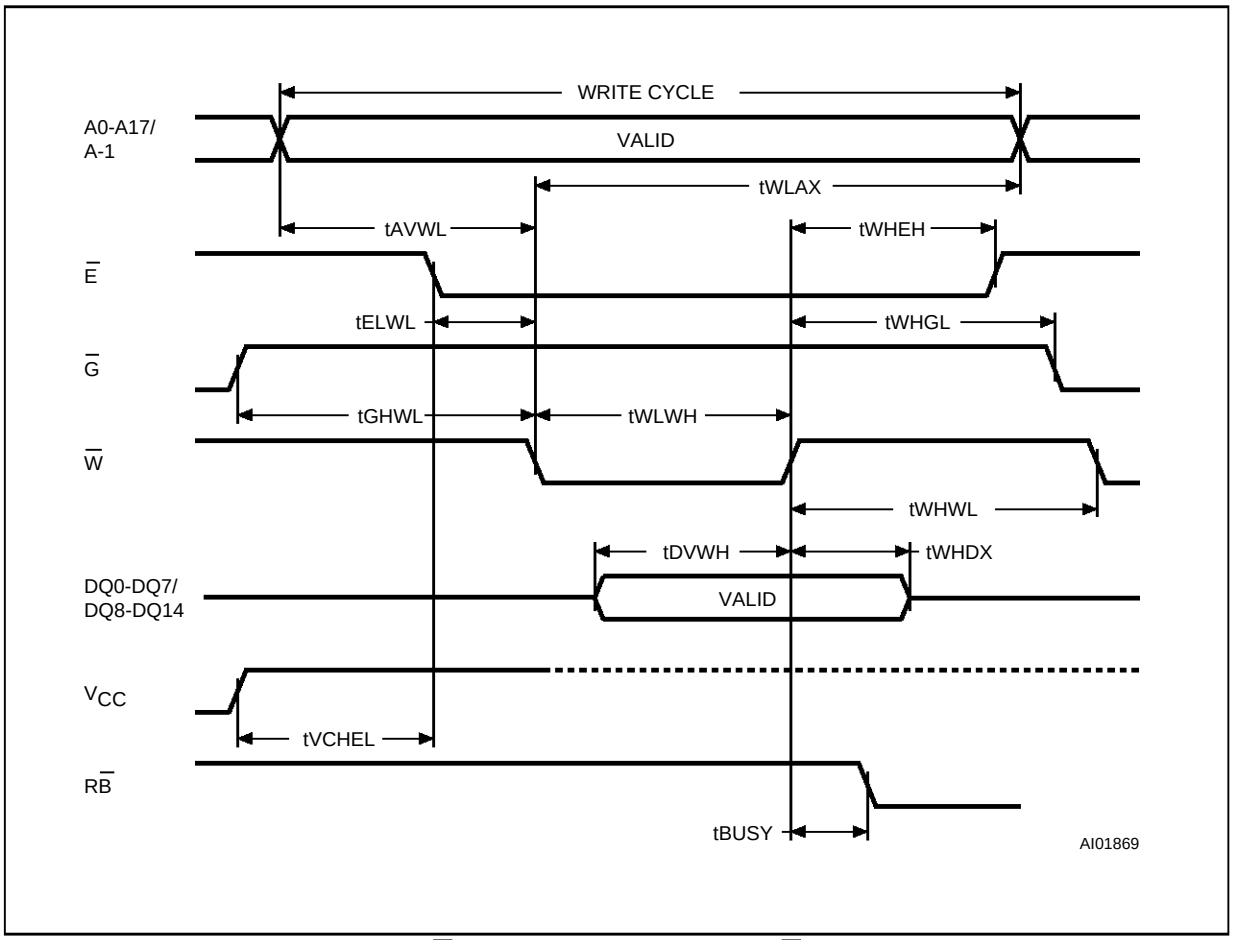
Symbol	Alt	Parameter	M29F400				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	10		10		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Block Erase)	1.5	30	1.5	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{VIDR} (2,3)		Rise TIme to V_{ID}	500		500		ns
t_{RP}		RP Pulse Width	500		500		ns
t_{BUSY} (2)		Program Erase Valid to $R\overline{B}$ Delay	30		35		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. Not 100% tested.
3. These timing are for Temporary Block Unprotected operation.

device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing to 0FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register bits. During the execution of the erase by the P/E.C., Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle Bits DQ2 and DQ6 toggle during erase operation and stop when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because the erasure has not been verified even after the maximum number of erase cycles have been executed.

Block Erase (BE) instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address 5555h on third cycle after the two coded cycles. The block Erase Confirm command 30h is written on sixth cycle after another two coded cycles. During the input of the second command an address within the block to be erased is given and latched into the memory. Additional block Erase confirm commands and block addresses can be written subsequently to erase other blocks in parallel, without further coded cycles. The erase will start after an Erase timeout period of about 100µs. Thus, addi-

Figure 7. Write AC Waveforms, $\overline{W}$ Controlled



Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

tional Block Erase commands must be given within this delay. The input of a new Block Erase command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Block Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C. is erasing the Block(s). If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the Block with 00h as the P/E.C. will do this automatically before to erasing to 0FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register status bits.

During the execution of the erase by the P/E.C., the memory accepts only the ES (Erase Suspend) and RD (Read/Reset) instructions. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle Bit DQ2 and DQ6 toggle during the erase operation. They stop when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because erasure has not completed even after the maximum number of erase cycles have been executed. In this case, it will be necessary to input a Read/Reset (RD) to the command interface in order to reset the P/E.C.

Table 16A. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -20 to 85°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F400				Unit
			-70 (4)		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	35		45		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	30		45		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	45		45		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		ns
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)	10		10		µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Block Erase)	1.5	30	1.5	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns
t_{VIDR} (2,3)		Rise TIme to V_{ID}	500		500		ns
t_{RP}		RP Pulse Width	500		500		ns
t_{BUSY} (2)		Program Erase Valid to $R\overline{B}$ Delay	30		35		ns

Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$
2. Not 100% tested.
3. These timing are for Temporary Block Unprotected operation.
4. At grade 1 (0 to 70°C) temperature range.

Program (PG) instruction. This instruction uses four write cycles. Both for Byte wide configuration and for Word wide configuration. The Program command A0h is written on the third cycle after two coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{E}$ and the Data to be written on its rising edge and starts the P/E.C. Read operations output the status bits after the programming has started. Memory programming is made only by writing '0' in place of '1' in a Byte.

Erase Suspend (ES) instruction. The Block Erase operation may be suspended by this instruction which consists of writing the command 0B0h without any specific address code. No coded cycles are required. It allows reading of data from another block and the programming in another block while erase is in progress. Erase suspend is accepted only during the Block Erase instruction execution. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the

Table 16B. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -20 to 85°C, -40 to 85°C or -40 to 125°C)

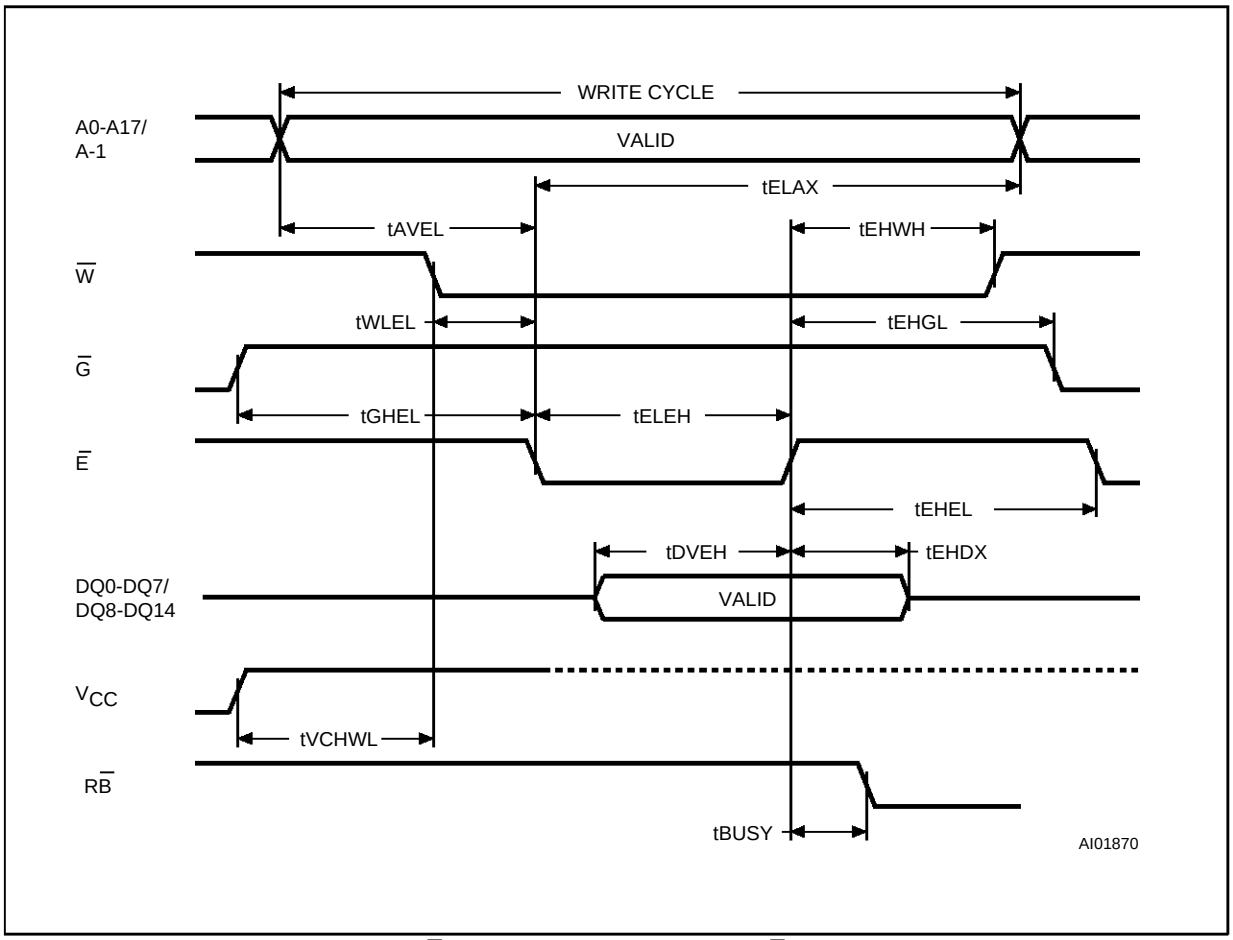
Symbol	Alt	Parameter	M29F400				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		ns
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)	10		10		µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Block Erase)	1.5	30	1.5	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns
t_{VIDR} (2,3)		Rise TIme to V_{ID}	500		500		ns
t_{RP}		RP Pulse Width	500		500		ns
t_{BUSY} (2)		Program Erase Valid to $R\overline{B}$ Delay	30		35		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. At grade 1 (0 to 70°C) temperature range.
3. Not 100% tested.

timeout. The Toggle Bit DQ2 and DQ6 stop toggling when the P/E.C. is suspended. Toggle Bits status must be monitored at an address other than in block being erased. Toggle Bits will stop toggling between 0.1µs and 15µs after the Erase Suspend (ES) command has been written. The M29F400T/B will then automatically set to Read Memory Array mode. When erase is suspended, Read from blocks being erased will output DQ2 toggling, Read from block not being erased is valid. During the suspension the memory will respond only to the Erase Resume (ER) instruction. A Read command will definitively abort erasure and result in invalid data in the Blocks being erased.

Program during Erase Suspend (PGES). The Program Instructions during Erase Suspend is allowed only on Blocks that are not Erase-suspended. This instruction uses four write cycles, both for byte wide configuration and for Word Wide configuration. The program command A0h is written on the third cycle after two coded cycles. A fourth write operation latches the Address on the falling edge of W or E and the Data to be written on its rising edge and starts the P/E.C. Read operations output the status bits after the programming has started. Memory programming is made only by writing '0' in place of '1' in a byte.

Figure 8. Write AC Waveforms, $\overline{E}$ Controlled



Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

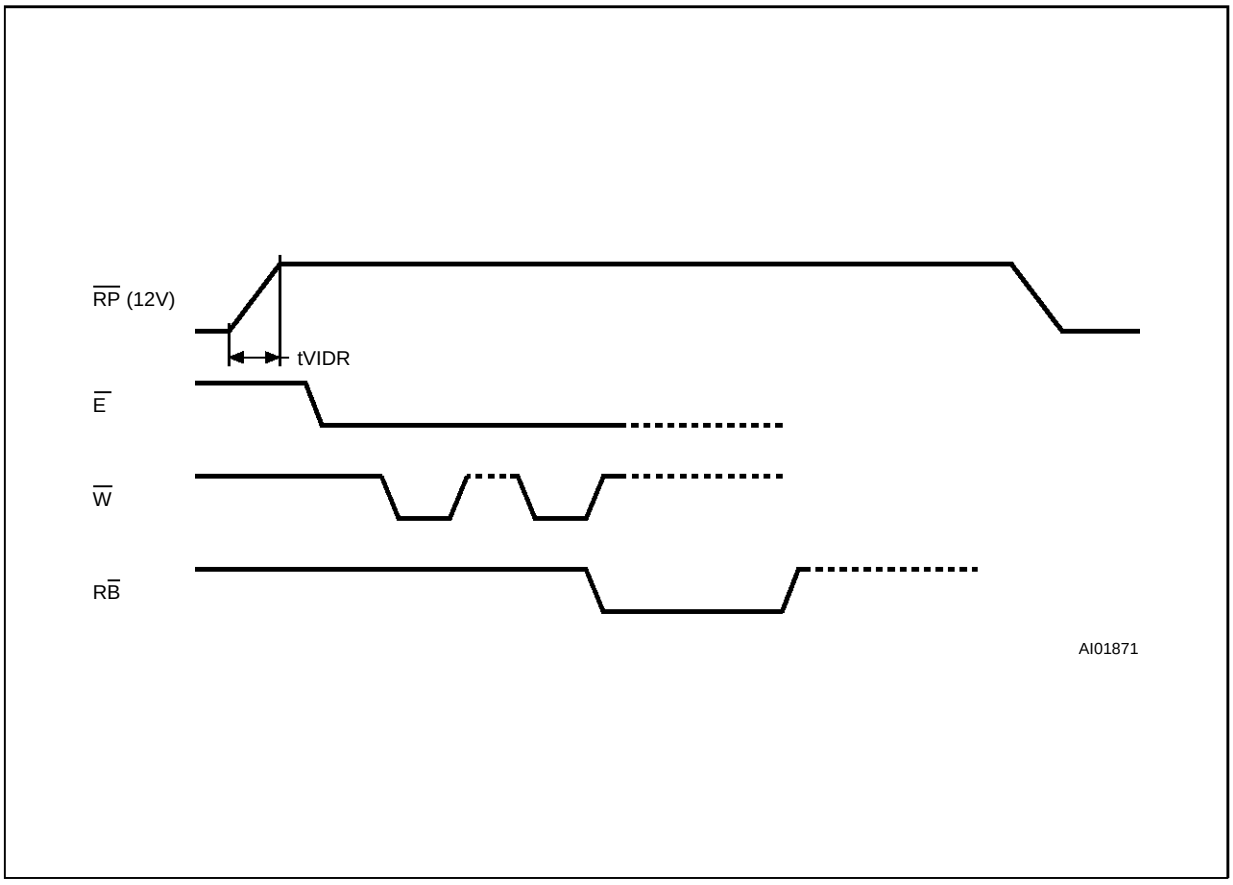
Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any coded cycles.

Power Down. The memory is Power Down when $\overline{RP}$ is at Low Level. The power comsumption is reduced to the Power Down level, and Outputs are in High Impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs. A Read/Reset command or $\overline{RP}$ at High Level will make the device exit from the Power Down mode. After 10µs the device will be ready for a new command sequence.

Programming. The memory can be programmed byte-by-byte or word-by-word. The program sequence is started by the two coded cycles, followed by writing the Program command (0A0h) to the Command Interface. This is followed by writing the address and data byte to the memory. The Program/Erase Controller automatically starts and performs the programming after the fourth write operation. During programming the memory status is checked by reading the status bits DQ2, DQ5, DQ6 and DQ7 which show the status of the P/E.C. DQ2, DQ6 and DQ7 determine if programming is on going or has completed and DQ5 allows a check to be made for any possible error.

Automatic Standby Mode. When the device is in active mode, with $\overline{E}$ at V_{IL}, and the addresses are unchanging for more than 150ns, an internal standby mode is activated. During this mode the power consumption falls to 30µA as a maximum. To recover the active mode the device can be accessed with standard access time (t_{CE}).

Figure 9. Temporary Block Unprotect Algorithm Waveforms, $\overline{W}$ Controlled



Power Up

The memory Command Interface is reset on power up to Read Array. Either $\overline{E}$ or $\overline{W}$ must be tied to VIH during Power Up to allow maximum security and the possibility to write a command on the first rising edge of $\overline{E}$ and $\overline{W}$. Any write cycle initiation is blocked when Vcc is below V_{LKO}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling; each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CC} program and erase currents required.

Table 17A. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C, -20 to 85°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F400				Unit
			-70 (3)		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled)	10		10		µs
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Block Erase, $\overline{W}$ Controlled)	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Chip Enable High to DQ7 Valid (Program, $\overline{E}$ Controlled)	10		10		µs
t_{EHQ7V2} (2)		Chip Enable High to DQ7 Valid (Block Erase, $\overline{E}$ Controlled)	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		30		35	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)	10		10		µs
t_{WHQV2}		Write Enable High to Output Valid (Block Erase)	1.5	30	1.5	30	sec
t_{EHQV1}		Chip Enable High to Output Valid (Program)	10		10		µs
t_{EHQV2}		Chip Enable High to Output Valid (Block Erase)	1.5	30	1.5	30	sec

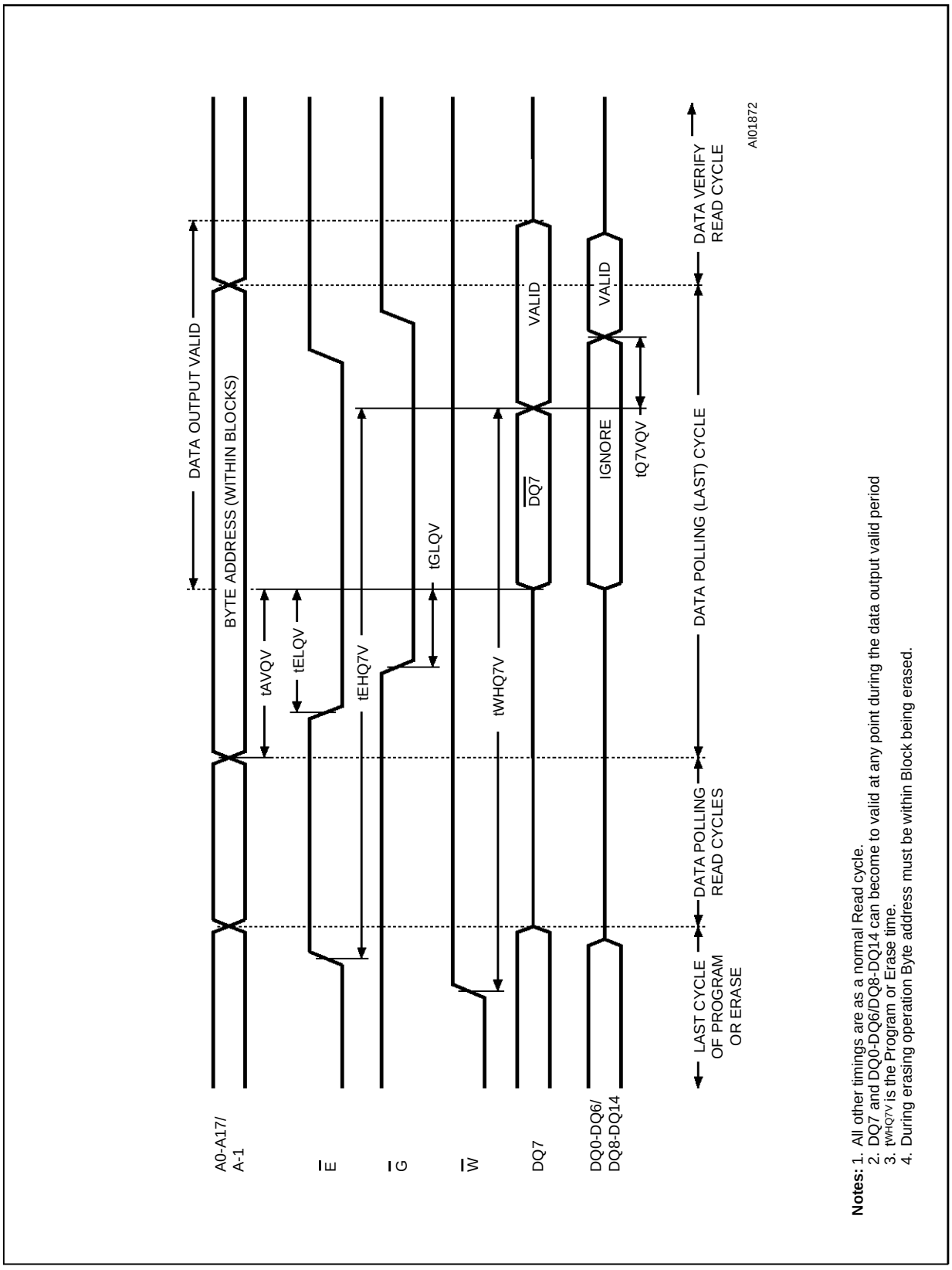
Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.
3. At grade 1 (0 to 70°C) temperature range.

Table 17B. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C, -20 to 85°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F400				Unit
			-120		150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled)	10		10		ms
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Block Erase, $\overline{W}$ Controlled)	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Chip Enable High to DQ7 Valid (Program, E Controlled)	10		10		ms
t_{EHQ7V2} (2)		Chip Enable High to DQ7 Valid (Block Erase, E Controlled)	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		50		55	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)	10		10		µs
t_{WHQV2}		Write Enable High to Output Valid (Block Erase)	1.5	30	1.5	30	sec
t_{EHQV1}		Chip Enable High to Output Valid (Program)	10		10		µs
t_{EHQV2}		Chip Enable High to Output Valid (Block Erase)	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Figure 10. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6/DQ8-DQ14 can become to valid at any point during the data output valid period
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Block being erased.

Figure 11. Data Polling Flow-chart

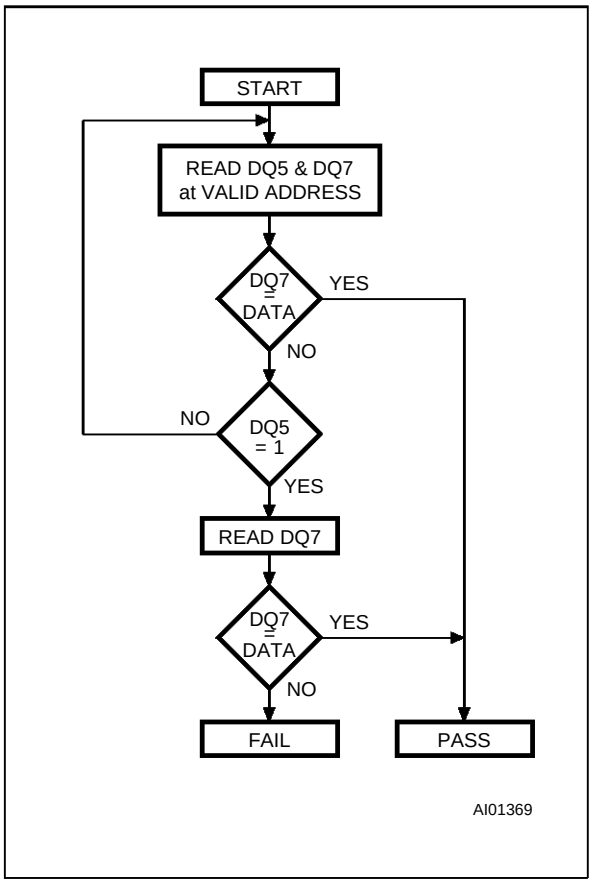
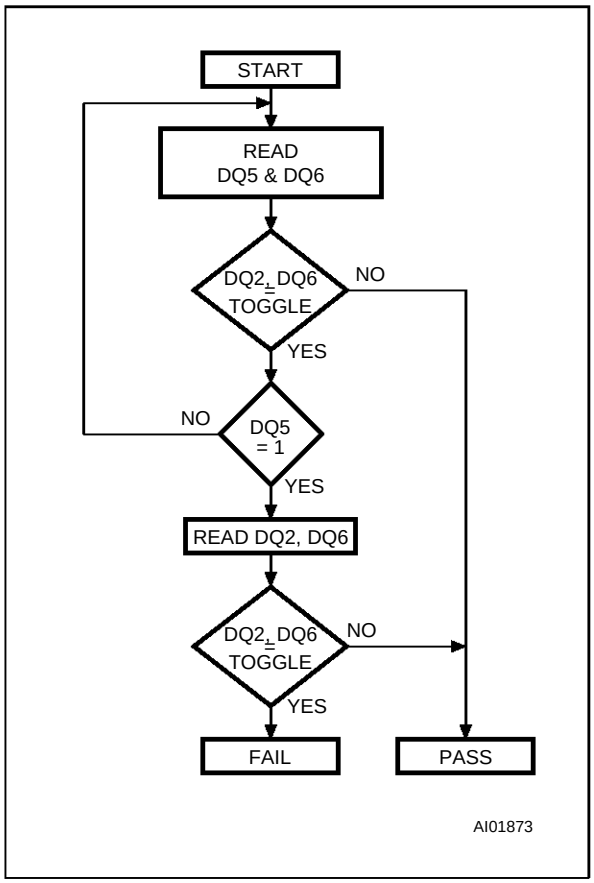


Figure 12. Data Toggle Flow-chart (1)

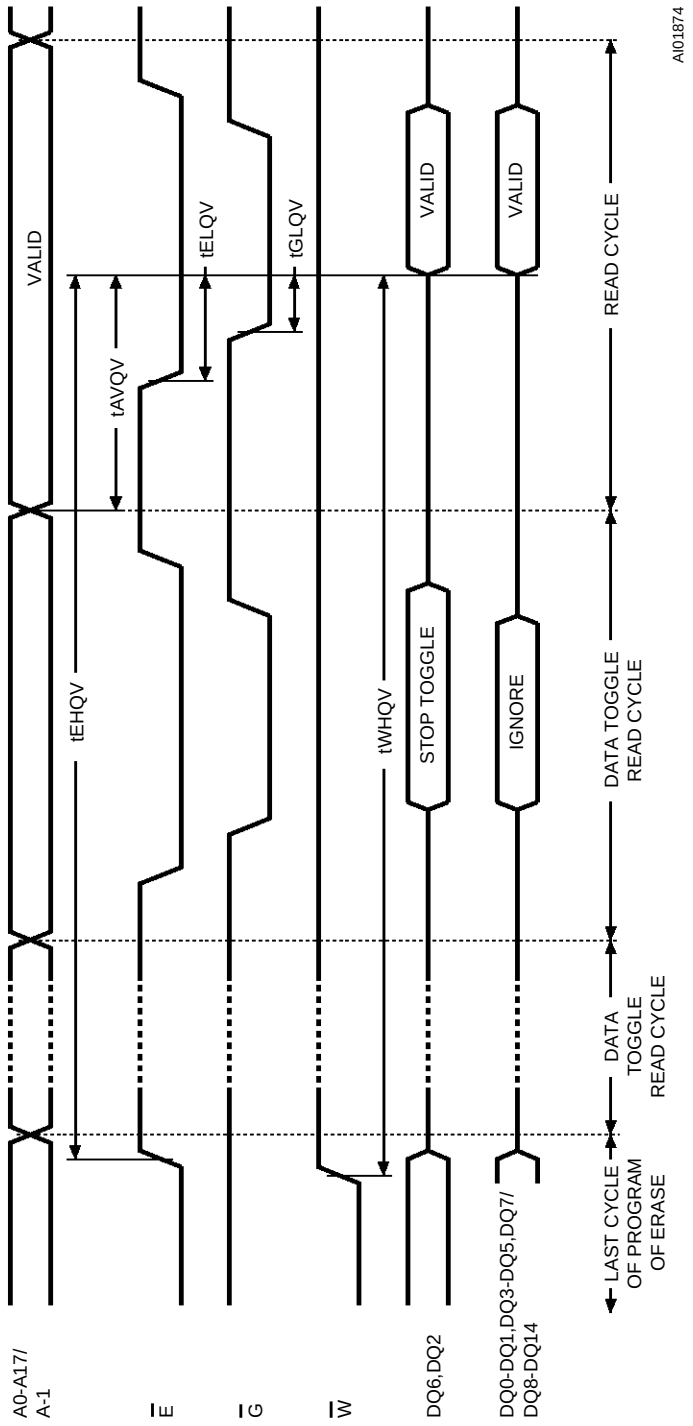


Note: 1. During Erase Suspend DQ2 will toggle together with DQ6.

Table 18. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = 0 to 70°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	M29F400			Unit
	Min	Typ	Max	
Chip Program (Byte)		8.5		sec
Bulk Erase (Preprogrammed)		2.5	30	sec
Bulk Erase		8.5		sec
Block Erase (Preprogrammed)		1	30	sec
Block Erase		1.5		sec
Byte Program		16	1200	µs
Word Program		16	2400	µs
Program/Erase Cycles (per Block)	100,000			cycles

Figure 13. Data Toggle DQ6, DQ2 AC Waveforms



Note: All other timings are as a normal Read cycle.

Figure 14. Block Protection Flow-chart

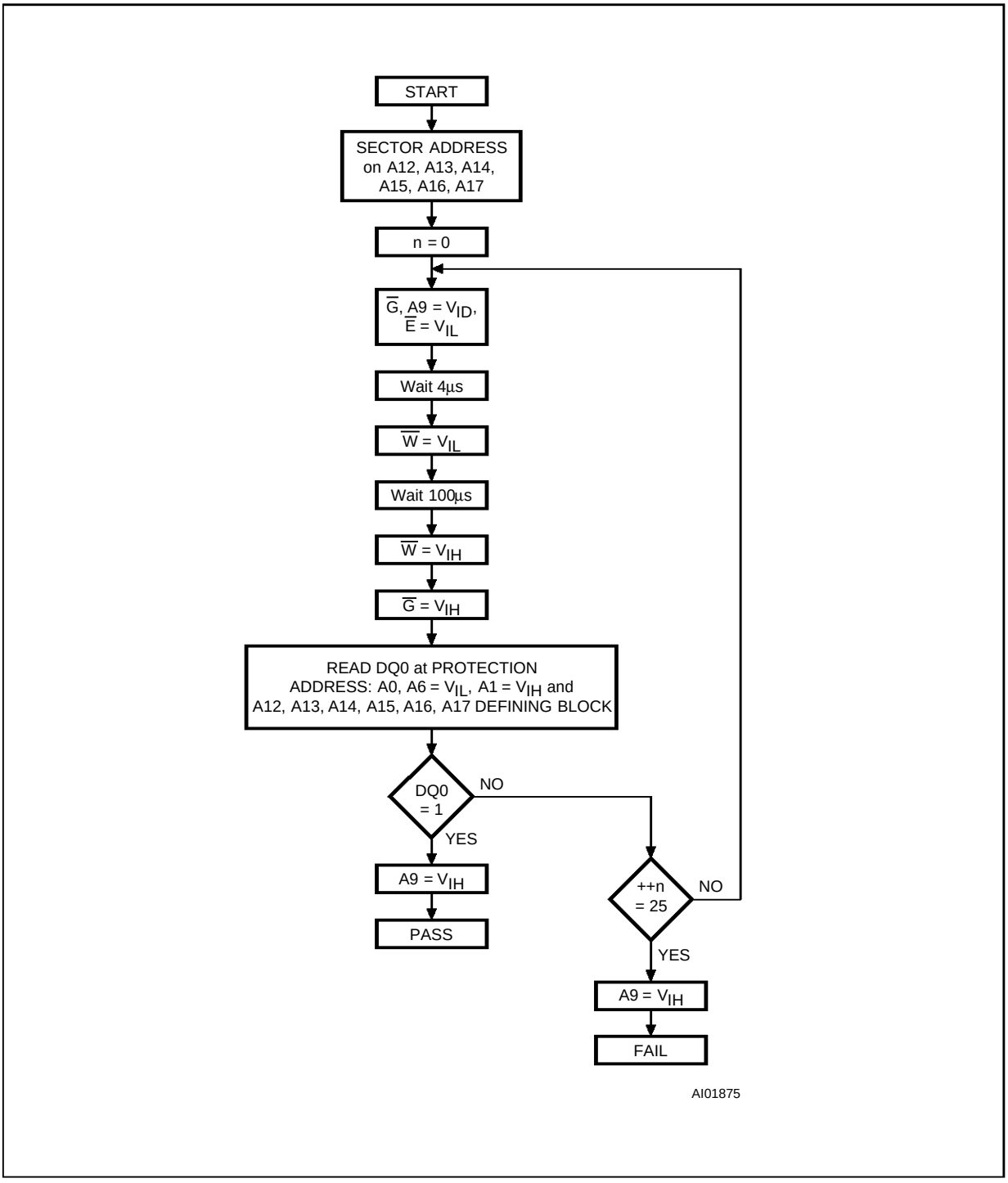
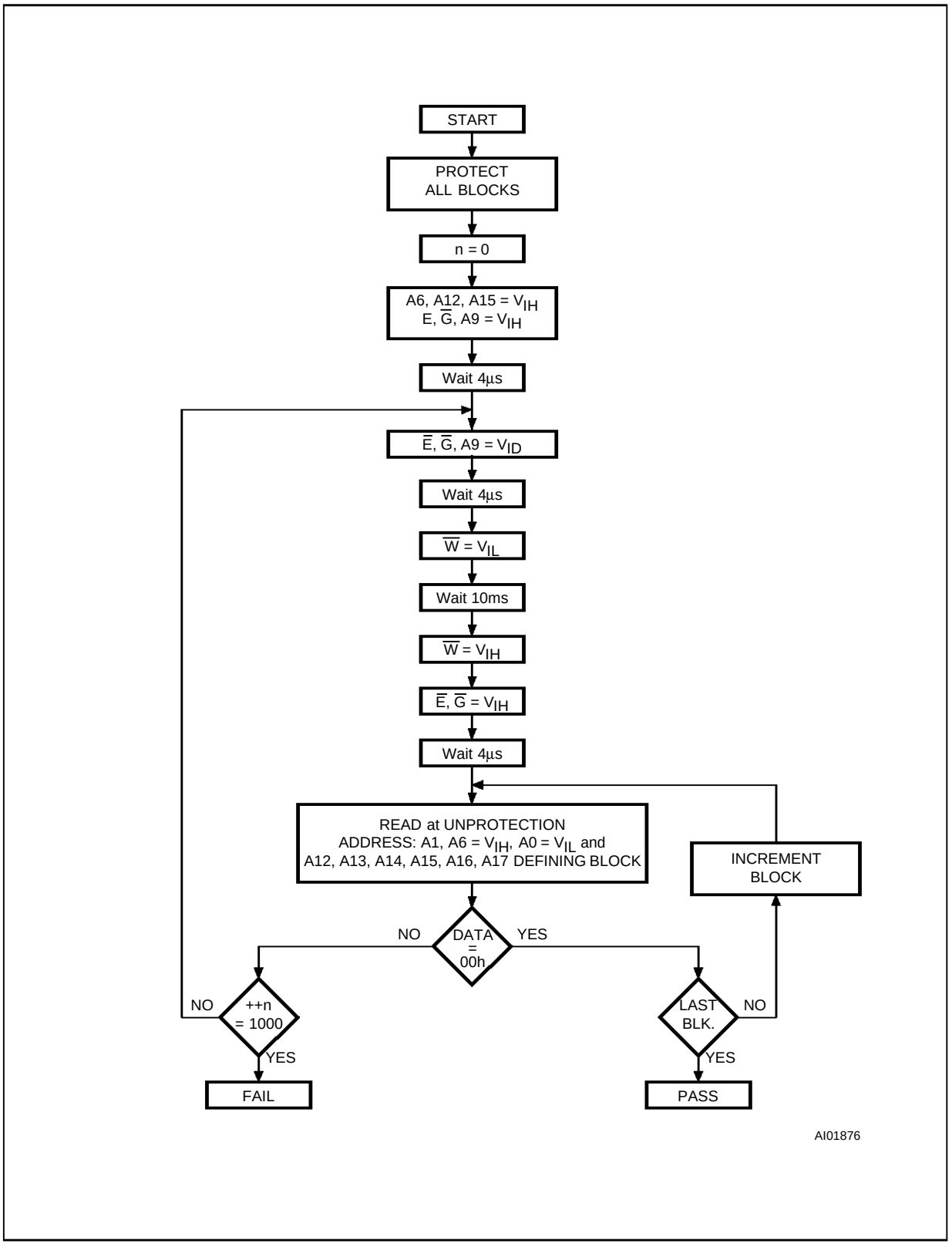
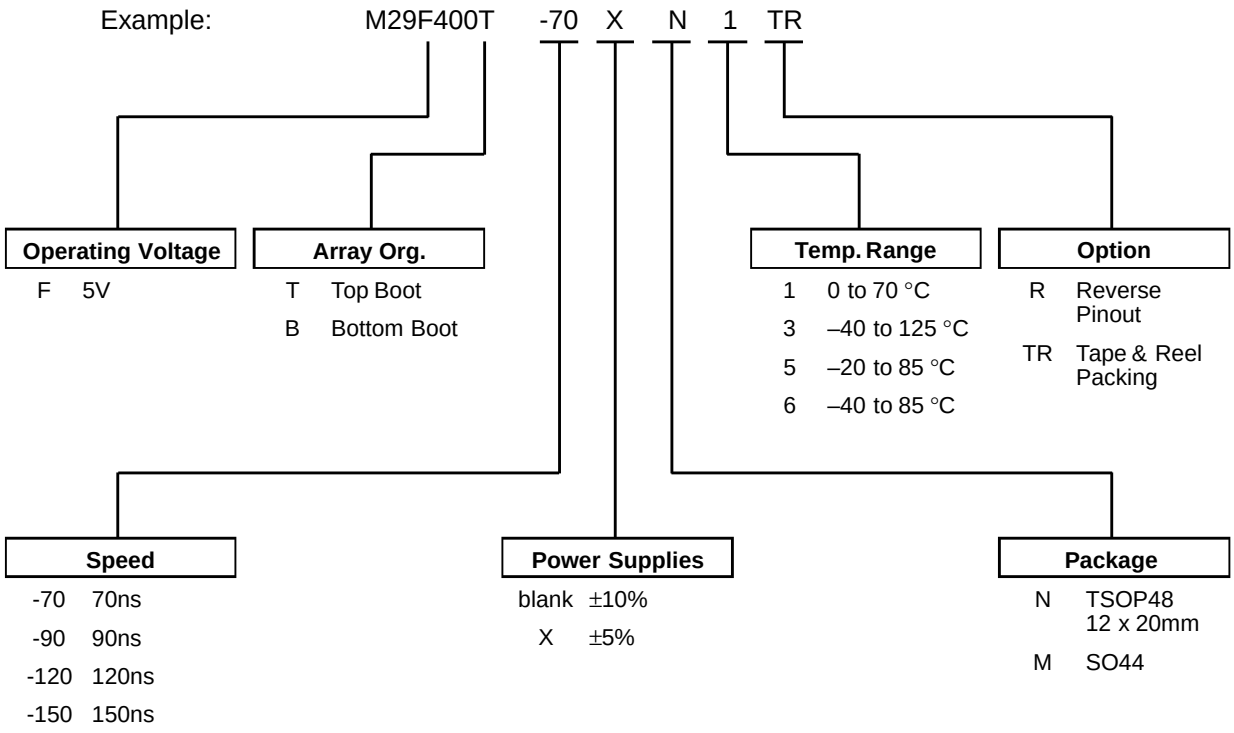


Figure 15. Block Unprotecting Flow-chart



ORDERING INFORMATION SCHEME



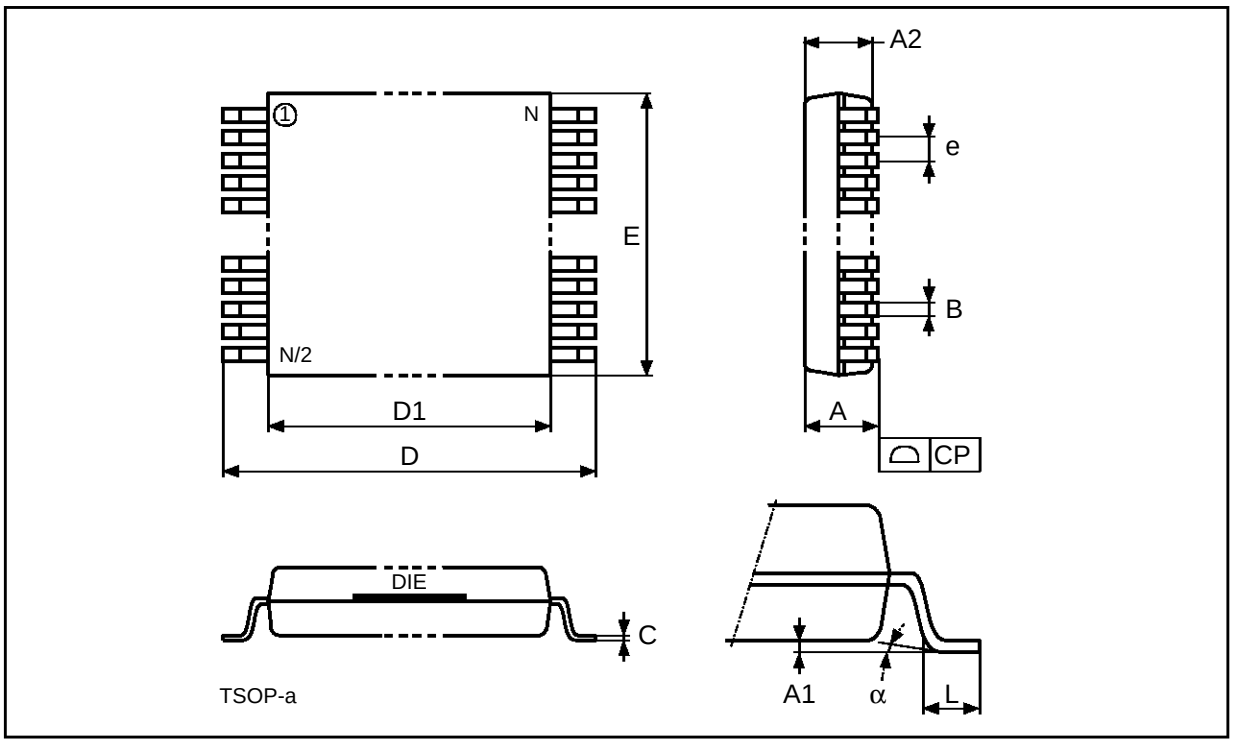
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

TSOP48 Normal Pinout - 48 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.004

TSOP48



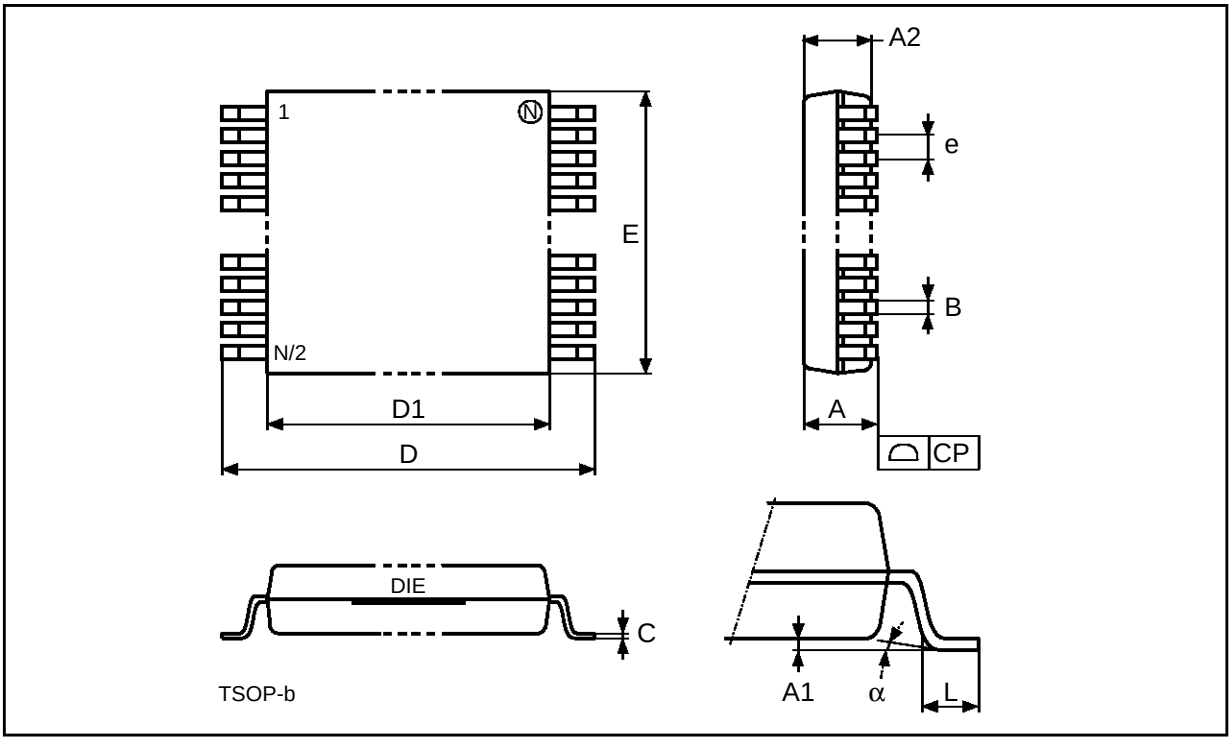
TSOP-a

Drawing is not to scale

TSOP48 Reverse Pinout - 48 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.004

TSOP48



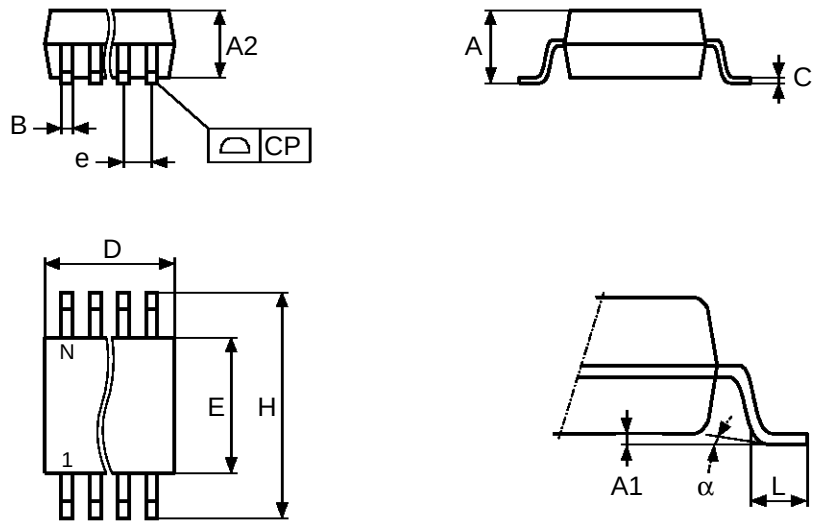
TSOP-b

Drawing is not to scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27			0.050		
H		15.90	16.10		0.626	0.634
L	0.80			0.031		
α	3°			3°		
N	44			44		
CP			0.10			0.004

SO44



SO-b

Drawing is not to scale